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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/923,997	08/07/2001	Hiroyuki Takahashi	SIM-01501	1911

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,997	TAKAHASHI, HIROYUKI	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15,22-24,29 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15* is/are allowed.

6)☒ Claim(s) *22-24,29 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the amendment filed 01/31/05. Applicant's arguments have been fully considered, but they are not persuasive.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 22-24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 22 is misdescriptive and rendered the claim indefinite. Claim 22 recite "a first capacitor having two electrodes, one of said electrodes connecting to a first power source line and the other connecting only to said first node. However, as seen in the drawing figure 2A shows that the second electrode of the capacitor P11 or P12 is connected to the both inverters V11 and V12 or to both V13 and V14.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 22 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by McClure (USP 5115146).

Insofar as understood to claim 22, McClure discloses in figure 1 a delay circuit (circuit comprises elements 12), comprising: first, second and third nodes; a first inverter (the second inverter from the left), the output of which coupled to the first node, the first inverter receiving a logic signal; a second inverter (the third inverter from the left), the input of which coupled to the first node and the output of which coupled to the second node; a third inverter (the fourth inverter from the left), the input of which coupled to the second node and the output of which coupled to the third node; a fourth inverter (the fifth inverter from the left), the input of which coupled to the third node; a first capacitor having two electrodes, one of said electrodes connecting to a first power source line and the other connecting only to said first node, first capacitor being a first transistor of a first channel type (p-type); a second capacitor coupled between the third node and the first power source line, the second capacitor being a second transistor of the first channel type; and wherein no capacitor is connected to the second node.

As to claim 23, figure 1 shows that the first transistor and the second transistor are P-MOS transistors, and the first power source line is fixed at a power potential.

5. Claims 22 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Watanabe et al. (USP 5055713) (previously cited).

As to claim 22, Watanabe et al. discloses in figure 11 a delay circuit (I9-I11 and NG), comprising: first, second and third nodes; a first inverter (I9), the output of which coupled to the first node, the first inverter receiving a logic signal; a second inverter (I10), the input of which coupled to the first node and the output of which coupled to the second node; a third inverter (I11), the input of which coupled to the second node and the output of which coupled to the third node; a fourth inverter (NG), the input of which coupled to the third node; a first capacitor

having two electrodes, one of said electrodes connecting to a first power source line and the other connecting only to said first node, first capacitor being a first transistor of a first channel type (n-type); a second capacitor (C3) coupled between the third node and the first power source line, the second capacitor being a second transistor of the first channel type; and wherein no capacitor is connected to the second node.

As to claim 24, figure 11 shows that the first transistor and the second transistor are n-MOS transistors, and the first power source line is fixed at a ground potential.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chaw (USP 5672990).

Chaw's figure 5 shows a delay circuit, comprising 2n+1 nodes (n=1; input node, ode between 30a, 30b, and node between 30b and 30c) defined in series, n being a natural number (n=1), a first node receiving a logical signal (input); 2n inverters (30a, 30b), each inverter arranged between adjacent nodes of the 2n+1 nodes; a capacitor coupled between an even node and a power source line (ground); and a NOR gate (30c) coupled to the first node and the (2n+1)th node. Thus, figure 5 shows all limitations of the claim except for the capacitor is NMOS transistor. However, it is notoriously well known that MOS capacitor is more compact than regular capacitor. Therefore, it would have been obvious to one having ordinary skill in the

art to use NMOS transistor connected as capacitor for Chaw's capacitor for the purpose of saving space.

8. Claim 32 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh et al. (USP 5764090) in view of Kubota et al. (USP 6492972).

Yeh et al.'s figure 10 shows a delay circuit receiving a logic signal (WE1) having a first logical level and a second logical level, comprising: a first inverter chain (611-613) including a plurality of inverters, said first inverter chain receiving the logic signal, a first logical gate (614) receiving the output of the first inverter chain and the logic signal; a second inverter chain (621, 622) including a plurality of inverters, the inverter chain receiving the output of the first logical gate; a second logical gate (623) receiving the output of the first logical gate and the output of the second inverter chain; and a third logical gate (631) receiving the logic signal and the output of the second logical gate. Thus, figure 10 shows all limitations shows all limitations of the claim except for each of the inverter chain further having a MOS capacitor. However, Kubota et al.'s figure 6 A shows that capacitor connected to inverter chain IV in order to increase the delay time of the inverter chain. It is also well known that MOS capacitor is more compact than regular capacitor. Therefore, it would have been obvious to one having ordinary skill in the art to add MOS capacitor to each of the delay chain for the purpose of increasing the delay time for the delay chain and for the purpose of saving space.

Allowable Subject Matter

9. Claim 15 is allowed.

Claim 15 is allowable because the prior art fails to teach or suggest that a gate threshold voltage of each gate of the P-MOS and n-MOS transistors is shifted in mutually opposing directions.

Response to Arguments

Applicant argues that McClure fails to teach "a first capacitor includes two electrodes, one of the electrodes connecting to a first power source line and the other connecting only to the first node". However, the claim is misdescriptive as stated above. Therefore, such limitation is not given patentable weight.

Applicant further argues that "Mcclure does not identify the capacitors 50 and 74 as transistors of a first channel type, as is claimed by Applicant". However, it is clearly seem in figures 1 and figure 2 that capacitors 46 and 74 are two different type of capacitors. One skill in the art would have recognized that capacitor 46 is N type capacitor and capacitor 74 is P type capacitor.

In response to the argument regarding to the rejection of claim 24, it is well known that the output of the NOR gate is low when the input of the NOR gate is high. Therefore, as broadest reasonable interpretation, the NOR gate is an inverter.

In response to the argument regarding to the rejection of claim 29, as stated above, NOR gate can be considered as inverter. Furthermore, it is seen as an intended use for NMOS capacitor for Chaw's capacitor. See other cited references.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 7, 2005

QUAN TRA
PRIMARY EXAMINER